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Fabrication of metal nanopatterns for organic field effect transistor electrodes by cracking and transfer printing

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Abstract

In this paper, we demonstrate a novel method for fabricating metal nanopatterns using cracking to address the limitations of traditional techniques. Parallel crack arrays were created in a polydimethylsiloxane (PDMS) mold using a combination of surface modification and control of strain fields. The elastic PDMS containing the crack arrays was subsequently used as a stamp to prepare nanoscale metal patterns on a substrate by transfer printing. To illustrate the functionality of this technique, we employed the metal patterns as the source and drain contacts of an organic field effect transistor. Using this approach, we fabricated transistors with channel lengths ranging from 70–600 nm. The performance of these devices when the channel length was reduced was studied. The drive current density increases as expected, indicating the creation of operational transistors with recognizable properties.

Supplementary material for this article is available online

Keywords: nanofabrication, crack, metal pattern, OFET, electodes

(Some figures may appear in colour only in the online journal)

1. Introduction

The ability to construct well-ordered metallic nanostructures over large areas has drawn great interest in recent years due to the increase in chemical detection and biosensing [1–3], optoelectronics [4], and particularly plasmonic applications such as surface plasmon resonance sensing [5] and surface-enhanced Raman scattering [6]. Several techniques have been developed for preparing metallic nanostructures on the surface of supporting substrates, including traditional micro/nanofabrication methods such as photolithography [7, 8], focused ion beam patterning [9, 10], and electron-beam writing [11]. However, these techniques typically have a low throughput, and incur a high cost for large area patterning, limiting their accessibility to non-specialist users. In addition, they are not suitable for use with many organic and biological species, or nonplanar substrates. Hence, more unconventional fabrication methods, such as soft lithography [12], nanoimprint lithography [13], wrinkling [14], and crack patterning [15] have emerged recently to address the limitations of traditional techniques. Of these unconventional methods, crack-based patterning has exhibited particular suitability for micro/nanofabrication [16], as it has been used in the preparation of nanowires [17], nanochannels [18], adsorbent surfaces [19], and flexible electronics [20]. A review of some applications of crack-based patterning is presented in [21].

The occurrence of cracks in materials is often random, and they are typically considered to be defects. Nevertheless, the mechanisms of crack generation and control have been studied to facilitate useful application of this phenomenon [22–26]. Arrays of cracks are formed in engineered structures when a brittle layer is supported on a substrate [27]. The characteristic features of these arrays depend on the geometry and properties of the brittle layer, the substrate interface, and the tensile strain [28]. Some researchers have intentionally generated cracks using inorganic materials, such as silicon nitride deposited on a silicon wafer [15, 29], by applying an appropriate amount of stress to the top layer. One of the deformation modes for hard materials, a 'crack',

is more difficult to manage than for soft materials due to its random generation and great complexity. Therefore, crack generation has been studied to understand its mechanism and to control cracking [30–35]. Recently, cracks on various hard, inorganic materials have been controlled on different length scales by using microtips [36] or notches [37]. Polymeric materials such as polydimethylsiloxane (PDMS) have also been used for intentional crack formation. It has been demonstrated that a distinct surface-modified layer, which is less than a micrometer thick, can be created through plasma oxidation or exposure to ultraviolet/ozone radiation [38]. Cracks can subsequently be formed on the oxidized layer by stretching, peeling, or swelling the PDMS bulk. However, the large modulus mismatch between this oxidized layer and the PDMS bulk results in crack arrays penetrating deep into the material, limiting the resolvable crack width to the microscale [18].

Therefore, a novel technique that can comprehensively and overcome the crucial limitations is strongly required for the practical application of the nanoscale crack method. In this paper, we report a method for creating metal nanopatterns using cracking and transfer printing. We created an oxidized layer on a surface by heating the PDMS bulk in ambient environment. An array of cracks is formed in this layer, followed by convex bending of the treated PDMS bulk. To control crack initiation at the desired position and orientation at microscopic scales, micro-notch structures, which concentrate stress to initiate cracks, were etched into the PDMS surface by laser scribing. The width of the cracks was in the nanoscale, and could be controlled by the heating time. The regular crack arrays were subsequently used as a stamp to fabricate metal nanopatterns by transfer printing. The nanoscale gaps between the deposited metal make these patterns suitable for use as the electrodes of an electronic device. We demonstrated this suitability by constructing organic transistors using the crack method. Accurate control of the geometric shape and dimensions of the nanopatterns is possible with this new method, resolving some of the limitations of previous crack-based techniques [19].

2. Experimental procedure

2.1. Stamp preparation

The PDMS bulk elastomer was prepared by mixing the monomer and cross-linking components from a Sylgard 184 kit (Dow Corning) in a 10:1 ratio. The resulting mixture was degassed, and cast on a glass slide, to a thickness of 1 mm. The entire system was then cured at 60 °C for 4 h, before the PDMS elastomer was peeled from the glass slide, and stored at room temperature until use. Then, the cured PDMS was cut into equal 1 cm × 1 cm pieces.

2.2. Reagents

Acetone, anhydrous ethanol and deionized water were used to clean the silicon and glass substrates. Polyvinyl alcohol (PVA) and poly(3-hexylthiophene-2,5-diyl) (P3HT) were purchased from Aldrich.

2.3. Cracks formation

The PDMS pieces were oxidized by heating at 400 °C for between 30 and 80 s, to generate a thin silica surface layer. The heating times were varied to control the final crack width. We applied a uniaxial stress by bending the PDMS pieces (1 cm × 1 cm × 1 mm) in a convex manner, such that the oxidized layer pointed outwards. The radius of curvature of the bent PDMS pieces was 0.1 cm. Multiple cracks were generated on the surface of the PDMS elastomer as a result of this bending. Figure 1(a) is a schematic diagram of the crack preparation process described above, with scanning electron microscopy (SEM) images of fabricated crack arrays shown in figure 1(b). The average crack spacing for 1 mm thick PDMS pieces is 60 μm.

We used a laser engraving machine to create micro-notch structures on the PDMS surface, which concentrate the stress applied to initiate crack formation in specific locations, as shown in the schematic illustration of crack formation (figures 2(a) and (b)). Then, the patterned PDMS was heated at 400 °C for 30 s to generate a thin silica surface layer. Cracks were generated on the surface of the PDMS elastomer as a result of bending.

2.4. Mechanical characterization

We analyzed the characteristics of the heat-treated PDMS substrate using tensile tests (Autograph AGS-X 1KN Shimadzu), nanoindentation tests (TI 950 TriboIndenter, Hysitron) and Fourier transform infrared (FTIR) spectroscopy (iN10MX, Nicolet). The three-dimensional structure of cracks was imaged using SEM (JSM-7500F, JEOL).

2.5. Fabrication of metal patterns by transfer printing

The fabricated crack arrays were used as molds for preparing metal nanopatterns. A 20 nm thick gold thin film was deposited onto the surface of a PDMS template using magnetic sputtering (Techno Corp., Beijing). A PVA water solution of 10% was then spin-coated onto a glass wafer (the spin-coated parameters were set as 1000 rpm for 30 s), and heated in an oven at approximately 80 °C for 2 min. The metal-coated PDMS stamp was subsequently reversibly bonded to the surface of the PVA-coated substrate, and the films were cooled to room temperature. As the adhesion of the gold thin film to the PVA is greater than it is to the oxidized PDMS layer, metal patterns were deposited on the substrate on separation from the PDMS bulk, in the regions where these materials were in direct contact. Following the transfer of the gold pattern, the only metal remaining on the PDMS stamp was located in the crack regions. This technique can be used to transfer metals other than gold from a cracked PDMS surface onto a polymer substrate. For polymers other than PVA, the spin-coated substrate should be heated to a value close to the glass transition temperature (T_g), if an amorphous material is used. For semi-crystalline polymers, the heating temperature is between T_g and the melting point (T_m).

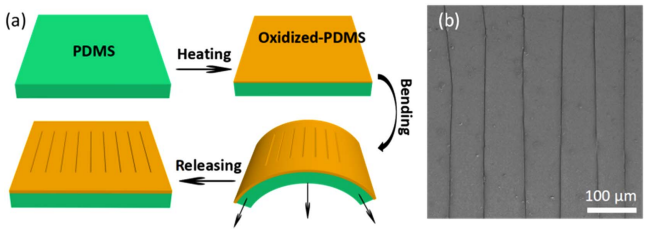

Figure 1. Novel method for fabricating parallel nanogaps using cracking. (a) Schematic illustration of the crack fabrication process. (b) SEM image of parallel quasi-periodic cracks on a PDMS surface.

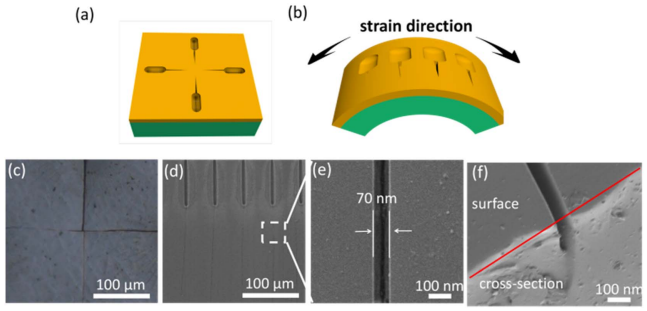

Figure 2. (a), (b) Schematic illustration of crack formation mediated by micro-notch structures. (c) SEM image of a cross-shaped crack. (d) SEM image of a parallel quasi-periodic crack array. (e) Enlarged partial SEM image of a fabricated crack. (f) SEM image of the cross-section of a crack.

2.6. Fabrication of transistor

We used a silicon wafer with a 300 nm thick silicon dioxide film ($\varepsilon_r = 3.9$, $C_i = 10\,\mathrm{nF\,cm^{-2}}$) as the gate electrode and the insulation layer for the organic field effect transistor (OFET), respectively. The SiO_2/Si wafer was divided into 25 mm × 25 mm pieces on which different transistor devices were fabricated. After cleaning the substrate successively with acetone, anhydrous ethanol, and deionized water, a 5 mm × 25 mm section of SiO_2 was removed using a reactive ion etching process performed in CF_4 gas, to expose a section of Si for testing the performance of the transistor. An $8\,\mathrm{mg\,ml^{-1}}$ solution of P3HT in chloroform was deposited onto the SiO_2/Si substrates via a spin-coating process. The P3HT-coated substrate was treated at 120 °C for 2 min, to facilitate an adhesive bond with the PDMS stamp. 30 nm thick source and drain electrodes were prepared by transferring gold from the PDMS stamp to the P3HT layer, in the manner described in section 2.5. Finally, after drying, the OFETs were annealed at 160 °C for 1 h to remove any moisture.

2.7. Characterization of OFETs

The characteristic output and transfer curves of the transistor were measured using a parameter analyzer (Keithley 4200 SCS America).

3. Results and discussion

3.1. Crack array formation and metal nanopattern transfer

Several factors determine the shape and width of cracks, such as the structure of the oxidized layer. In this section we provide an analysis of some of these parameters.

Figures 2(a) and (b) are schematic diagrams depicting micro-notch-guided crack generation, illustrating that crack formation can be controlled using the shape of micropatterns on the surface of the oxide layer. This control is possible because the geometry of the oxide layer regulates the strain fields at the tip of the notches. Cracks are consequently developed along the direction of the notch structures. We defined different micro-notch structures on the PDMS surface using laser ablation, for the generation of cross-shaped cracks (figure 2(c)), and long straight crack arrays with a uniform 50 μm-pitch (figure 2(d)). The PDMS was oxidized by heating at 400 °C for 30 s. In this experiment condition, the three-dimensional structure of the resulting cracks can be elucidated from the enlarged SEM image in figure 2(e), and the cross sectional SEM image in figure 2(f). The width of a crack was measured to be approximately 70 nm, and the depth was approximately 100 nm. Parallel quasi-periodic linear crack arrays were fabricated on a PDMS surface using this novel method, providing new opportunities for large-scale device construction.

The mechanical characteristics and thickness of the oxidized layer are also significant factors that alter the cracking response, as the orientations and shapes of cracks in the layer atop the PDMS substrate are determined by the interfacial stress between the different materials. A comparison of the mechanical properties of the oxide layer and PDMS after heating (obtained from tensile and nanoindentation tests) indicated that the surface layer was stiffer and more brittle than the bulk (figure S1 is available online at stacks.iop.org/NANO/29/145301/mmedia in the supporting information section). The changes in bulk modulus and toughness data thus suggest that for the purposes of crack formation, the oxide layer and the PDMS bulk can be treated as different materials. We performed FTIR analysis in attenuated total reflection mode (FTIR-ATR) to reveal the chemical functionality of PDMS. Our analysis reveals that heat oxidation treats PDMS to a depth of several micrometers. Unmodified PDMS exhibits a series of characteristic IR bands (table S1 in the supporting information). The FTIR-ATR spectra in figure 3(a) show a decrease in the intensity of the band representative of the Si–O–Si signal (band 5) with increases to heating time, indicating the occurrence of chain scission in the PDMS network. There is also a simultaneous decrease in the intensity of $-CH_3$ signals (bands 1, 7, and 8), which is accompanied by an increase in the intensity of the $-OH$ signal (bands 2 and 3). This phenomenon is suggestive of oxidative conversion of $-[(CH_3)_2Si–O]-$ molecules into more hydrophilic species. From these results, we conclude that modifications from heat treatment propagate deeper into the PDMS substrate with increasing time, causing irreversible chemical changes to the surface region. These changes create a silica-like layer on the PDMS surface that becomes stiffer and more brittle with increased heating time. We varied the heating time between 30 and 80 s, and monitored the effects on the

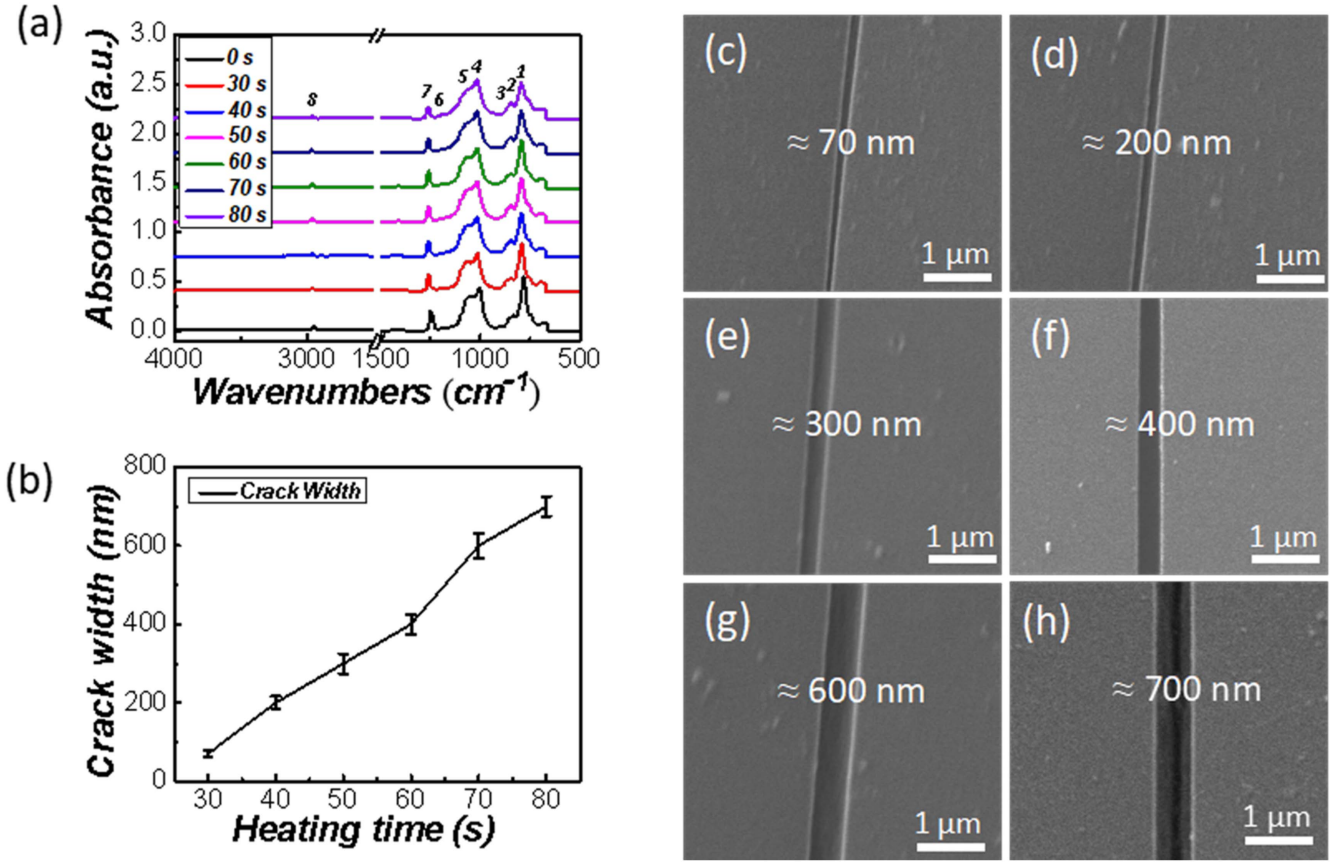

Figure 3. (a) FTIR-ATR spectra of PDMS heat-treated at 400 °C for varying lengths of time (0, 30, 40, 50, 60, 70, and 80 s). (b) Plot illustrating average crack width as a function of heating time. (c)–(h) SEM images illustrating the variation in the crack width of samples as a function of heating time (30, 40, 50, 60, 70, and 80 s, respectively).

cracks generated. Figure 3(b) shows that the crack width increases proportionally with the heating time, illustrating that this parameter can be used to control crack formation. Examples of cracks generated with different heat-treatment durations are shown in figures 3(c)–(h), and the supporting information (figure S2).

Following the generation of these crack arrays, we constructed a metal array on a polymer-coated substrate corresponding to the patterns of the selected template by transfer printing (see figure 4(a)). The printing mechanism is based on the difference in adhesion between the gold thin film, the PDMS stamp, and the substrate [39]. We selected the template that oxidized by heating at 400 °C for 30 s. Figure 4(b) is an enlarged image of the gap between metallic patterns, which is approximately 70 nm. This image reveals that the edge of the gap is well defined, highlighting the fidelity of the technique. In addition, the PDMS substrate can be recycled after peeling off the metal. We studied the metal patterns after transfer printing 3, 5, 7 and 10 times. The metal patterns are still clear and regular, as shown in figure 4(c)–(f).

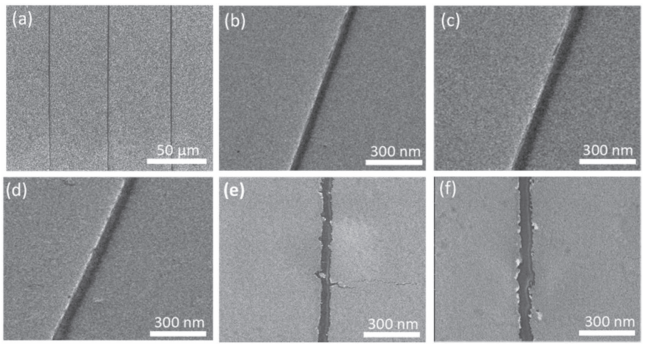

Figure 4. (a) Metal nanopattern deposited on a substrate. (b) Enlarged image of the gaps between the nanopattern in (a). (c)–(f) are metal patterns obtained from the third, fifth, seventh and tenth transfer printing.

3.2. P3HT OFET

Fabricating a short-channel device has been proven to be an effective approach for improving the performance and reducing the power consumption of electronics based on semiconducting polymers, where the mobility of charge carriers is poor. For instance, reducing the distance between the source-drain electrodes of an OFET was found to significantly increase the transit frequency and the drive current per unit area [40]. There is growing interest in the use of OFETs for inexpensive electronics, due to the increased prevalence of methods for creating metal nanopatterns in large areas.

We investigated the performances of top-contact polymer nanoscale-channel OFETs with crack-patterned electrodes (figure 5(a)). As we used a size-defined mask when depositing

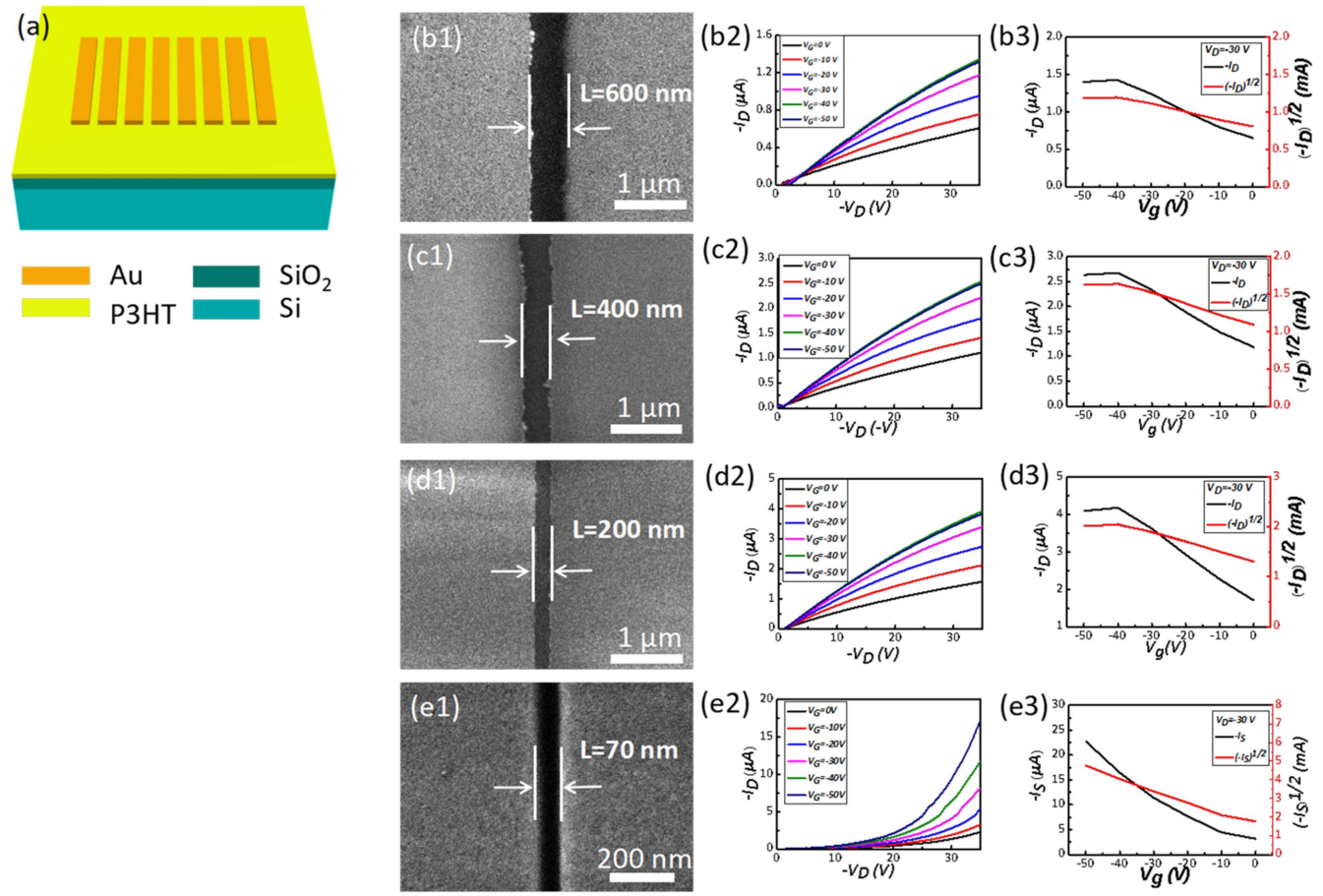

Figure 5. (a) Illustration of an OFET. Typical performance of P3HT OFET devices with channel lengths of (b) 600 nm, (c) 400 nm, (d) 200 nm, and (e) 70 nm. The output characteristics of the devices were measured with gate voltages varied between 0 and −35 V. The transfer characteristics of the devices were measured at a drain voltage of −30 V.

the metal on the PDMS template, all electrodes were 5 mm wide. The lengths of the channels were modified using the cracks in the PDMS stamp, by controlling the duration of heat treatment. Figures 5(b)–(e) show the performance of P3HT devices with channel lengths of approximately 600 nm, 400 nm, 200 nm, and 70 nm, prepared with heating times of 70, 60, 40, and 30 s, respectively.

All device measurements were performed in atmosphere using a Keithley 4200 SCS analyzer. The measured *I–V* curves of typical P3HT devices with channel lengths between 600 nm and 200 nm (figures 5(b)–(d)) are characteristic of a p-channel transistor. At these longer channel lengths, the devices demonstrated standard FET characteristics as the drain current (I_D) increased as the channel length (L) was reduced. An analysis of the experimentally derived characteristics of these devices indicates that their behavior is in agreement with Poole–Frenkel theory [41].

As the channel length is decreased to 70 nm, the observed behavior deviates significantly from that of a standard OFET. It can be seen in figure 5(e) that 70 nm devices are no longer capable of saturation, and instead demonstrate a continuous increase in I_D with V_D. This phenomenon is the short-channel effect, observed as a parabolic source-drain *I–V* characteristic with respect to a fixed V_G, without a saturation region. For channel lengths below 200 nm, the I_D no longer displays a shape that is typical of the output characteristic of an OFET, even if V_G modulation can still be observed. Although the inability to saturate is widely observed in short-channel OFET devices [41, 42], reported explanations for this phenomenon vary.

Carrier mobility was determined in the fabricated P3HT transistors based on the following relationship for operation in saturation:

$$I_D = \mathrm{W}C_i\mu(\mathrm{V}_G - \mathrm{V}_T)^2/2\mathrm{L} \quad (1)$$

where I_D is the drain current, V_G is the gate voltage, and W and L are the channel width and channel length, respectively, as defined previously. μ is the carrier mobility, C_i is the capacitance per unit area, and V_T is the threshold voltage. At a drain-source voltage of −30 V, the mobilities of the devices characterized in figures 5(b)–(d) were calculated to be 3.75×10^{-6}, 4.88×10^{-6}, and 5.98×10^{-6} $\mathrm{cm}^2\ \mathrm{V}^{-1}\ \mathrm{s}^{-1}$, respectively. A comparison of these mobilities with that of the transistor characterized in figure 5(e) is difficult, as short-channel devices do not saturate. The on/off current ratios of the transistors were poor; approximately 2.3, 2.5, 2.7 and 6.4 for the patterned devices. It is noted that both the on/off current ratios and mobilities values obtained in the our present work are low compared with those reported in the literatures [43–45]. We suggest that the P3HT might have been doped

with oxygen, moisture or impurities for devices fabricated and measured in ambient conditions. We are sure that employing the processes with special surface or heat treatment, an inert environment during the transfer printing Au electrode and electrical measurements in vacuum will provide greatly enhanced electrical properties.

4. Conclusion

In summary, we have demonstrated a new procedure for fabricating metallic nanostructures using a tunable crack formation process. The fabrication procedure consists of the deposition of a thin metal film on a PDMS stamp defined by crack formation, followed by transfer printing of the metal nanostructures in the final patterning step. The proposed technique is a simple and controllable methodology, and presents many advantages, such as cost reduction, time optimization, suitability for modifying large areas, and simultaneous production of micro/nano-patterns. In addition, the technique can be used to create a wide range of channel dimensions, with widths varying between 70–600 nm, demonstrating the tunability of the process. These advantages make the nanofabrication approach very useful for manufacturing next-generation optoelectronic devices, particularly those used in flexible and stretchable organic electronics.

Acknowledgments

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Conflicts of interest

There are no conflicts to declare.

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